ABSTRACT OF THE DISCLOSURE

A system and method for coordinating synchronizer controllers disposed in different clock domains, e.g., a core clock domain and a bus clock domain, wherein a clock synchronizer arrangement is employed for effectuating data transfer across a clock boundary therebetween. A bus clock synchronizer controller operable in the bus clock domain includes circuitry for generating a set of inter-controller clock relationship control signals, which are provided to a core clock synchronizer controller. Responsive to the inter-controller clock relationship control signals, circuitry in the core clock synchronizer controller is operable to synchronize the core clock signal's cycle and sequence information relative to the bus clock signal.